

Docket No.: 0885-CS



2816  
Election #10  
PATENT  
4/17/00  
[Signature]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Joel PAGE, et al.

Serial No.: 09/153,864

Group Art Unit: 2816

Filed: September 16, 1998

Examiner: J. Zweizig

For: POWER ON RESET TECHNIQUES FOR AN INTEGRATED CIRCUIT CHIP

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**RESPONSE TO RESTRICTION REQUIREMENT**

Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

This is in response to the Examiner's Restriction Requirement of March 15, 2000.

The Examiner required restriction to one of the following inventions under 35

U.S.C. 121:

I. Claims 1-13, drawn to a power ON reset circuit, classified in class 327, subclass 143;

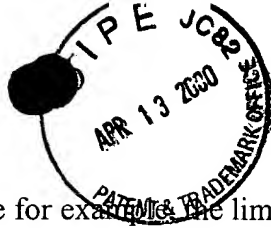
II. Claims 14-17, drawn to a memory device, classified in class 395, subclass 500.

Applicants hereby elect the claims of Group 1, namely claims 1-13, drawn to a power ON reset circuit. However, that election is undertaken with traverse.

The Examiner is respectfully requested to reconsider the Restriction Requirement.

The claims of Group II are Beauregard claims that are very much related to the claims of

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the Group I set. Compare for example the limitations of claim 14 with the limitations of claim 7. The similarity of the inventions becomes clear.

Accordingly, the Examiner is requested to reconsider the Restriction Requirement and withdraw it.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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